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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,532	10/12/2000	Navaz Lulla	0325.00420	9027

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EXAMINER	
WHITMORE, STACY	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/689,532	LULLA ET AL.	
	Examiner	Art Unit	
	Stacy A Whitmore	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3, 5-10, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter referred to as IEEE Std 1149.1).

2. "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" was cited on the IDS dated 12/26/00.

3. As for claim 1, IEEE Std 1149.1 taught the invention as claimed, including an apparatus comprising:

a circuit configured to select one of a number of identification codes (ID) codes in response a voltage level at one or more pins [pg. 11, section 3.5, "TDO"; pg. 56, section 7.12.1 and 7.12.2; pg. 107-108, section 11. device ID register; pg. 108, sections 11.1.1 d and e, fig. 11-1; pg. 109, first three paragraphs; the binary values/ logic levels at the pins of the device ID register inherently represent a voltage level at one or more pins, see also applicant disclosure, pg. 6, TDO is the output selection].

4. As for claim 2, IEEE Std 1149.1 further taught wherein said ID code is a silicon ID of an electronic part [pg. 108, fig. 11-1; pg. 111, section 11.3.1].

5. As for claim 3, IEEE Std 1149.1 further taught wherein said number of ID codes are programmed using one or more options selected from the group consisting of metal options, bond options, and hard coded options [pg. 55, section 7.11, fuse programmable reads on hard coded/metal options , see applicant's specification, pg. 26, lines 1-3, and also pg 6, lines 7-9 where hard coded/ metal options are described].

6. As for claim 5, IEEE Std 1149.1 further taught wherein said ID code comprises a part number for said apparatus [pg. 108, fig. 11-1; pg. 111, section 11.3.1].

7. As for claim 6, IEEE Std 1149.1 further taught wherein said ID code (part number) is combined with other identification codes [pg. 108, fig. 11-1].

8. As for claim 7, IEEE Std 1149.1 further taught wherein said other ID codes comprise one or more codes selected from the group consisting of a version number and a manufacturer number [pg. 108, fig. 11-1].

9. As for claim 8, IEEE Std 1149.1 further taught wherein said ID code is captured in a register [pg. 56, section 7.12.1, element c].

10. As for claim 9, IEEE Std 1149.1 further taught wherein said register comprises a JTAG ID code register [pg. 56, section 7.12.1, element c; and pg. iii, JTAG].

11. As for claim 10, IEEE Std 1149.1 further taught wherein said apparatus comprises a programmable logic device (PLD) [pg. 104, section 10.8.2 programmable component; and pg. 112, section 12.2.2, component].

12. As for claim 20, IEEE Std 1149.1further taught an apparatus comprising:

means for generating a number of identification codes in response to a voltage level asserted at one or more pins; and means for determining a voltage level to assert at one or more pins [pg. 11, section 3.5, "TDO"; pg. 56, section 7.12.1 and 7.12.2; pg. 107-108, section 11. device ID register; pg. 108, sections 11.1.1 d and e, fig. 11-1; pg. 109, first three paragraphs; the binary values/ logic levels at the pins of the device ID register inherently represent a voltage level at one or more pins, see also applicant disclosure, pg. 6, TDO is the output selection].

13. Claims 1, 3-4, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ulchida (US Patent 5,467,304)

14. As for claim 1, Uchida taught the invention as claimed, including an apparatus comprising:

a circuit configured to select one of a number of identification codes (ID) codes in response a voltage level at one or more pins [col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19, and col. 5, lines 23-30, and col. 6, lines 14-33].

15. As for claim 3, Uchida further taught wherein said number of ID codes are programmed using one or more options selected from the group consisting of metal options, bond options, and hard coded options [col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19, and col. 5, lines 23-30, and col. 6, lines 14-33].

16. As for claim 4, Uchida further taught wherein said one or more pins are connected to either a voltage supply power or a voltage supply ground according to package markings [col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19, and col. 5, lines 23-30, and col. 6, lines 14-33; diffusion of bonding pads of the kinds of circuit corresponds to package markings].

17. As for claim 12, Uchida further taught wherein said bond options are set based on a package of said apparatus [col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19, and col. 5, lines 23-30, and col. 6, lines 14-33; diffusion of bonding pads of the kinds of circuit corresponds to package markings].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 16, and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" in view of "Supplement to IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture" (hereinafter referred to as Supplement).

19. "Supplement to IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture" was cited on the IDS dated 12/26/00.

20. As for claims 16, IEEE Std 1149.1 taught the invention substantially as claimed, including a method of selecting one of a number of ID codes comprising the steps of:

(a) asserting a first or a second voltage level on one or more pins of said package; and (b) generating said one of a number of ID codes in response to said voltage levels on said one or more pins [see as cited in the rejection of claim 1].

IEEE Std 1149.1 did not specifically teach a single die and package combination. However, Supplement taught a single die and package combination [pg. 3, section B.2, pg. 12, fig B-1, and section B.8.2]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of IEEE Std 1149.1 and Supplement because Supplement is an additional revision adding more functionality to the existing IEEE Std 1149.1 which improves on the original IEEE Std 1149.1 standard and would further be obvious to one of ordinary skill in the art to utilize published IEEE standards for the development of additional device functions taught by the IEEE standard.

21. As for claim 18, IEEE Std 1149.1 further taught the step of:

c) presenting said ID code in response to an identification request [see as cited in the rejection of claim 1, see also, pg. 55-56, IDCODE and USERCODE instructions which are the requests].

22. As for claim 19, IEEE Std 1149.1 further taught wherein said ID request comprises a JTAG ID code instruction [see as cited above in the rejection of claim 18].

23. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" in view of Carmichael et al. (US Patent 6,308,311).

24. As for claim 11, IEEE Std 1149.1 taught the invention substantially as claimed, including the apparatus as cited in the rejection of claims 1 and 3 with respect to the rejections made with the IEEE Std 1149.1 reference. IEEE Std 1149.1 did not specifically teach wherein said metal options are set to indicate an operating voltage of said apparatus. However, Carmichael taught wherein device ID options are set to indicate an operating voltage of said apparatus [col. 12, line 67 – col. 13, line 4]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of IEEE Std 1149.1 and Carmichael because setting IEEE Std 1149.1's metal options with an operating voltage of said apparatus would IEEE Std 1149.1's identify devices for proper operating characteristics and avoid potential damages to devices [see Carmichael, col. 13, lines 15-18].

25. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US Patent 5,467,304) in view of Carmichael et al. (US Patent 6,308, 311).

26. As for claims 13 and 14, Uchida taught the invention substantially as claimed, including the apparatus as cited in the rejection of claim 1 where Uchida was cited as

the reference. Uchida did not specifically teach wherein said pins are labeled as either a first or second supply voltage/based on characteristics of said apparatus. However, Carmichael taught wherein pins are labeled either a first or second supply voltage based on characteristics of an apparatus [col. 12, line 66 – col. 13, line 4]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida and Carmichael because adding a pin labeled as a first or second supply voltage to Uchida's system would have improved Uchida's system by allowing Uchida's system to adjust operating characteristics (e.g. supply voltage) of different devices, and thereby prevent possible damages due to incorrect supply voltages [see Carmichael, col. 12, lines 45-48].

27. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US Patent 5,467,304) in view of Carmichael et al. (US Patent 6,308, 311), and further in view of Wegner et al. (US Patent 6,311,246).

28. As for claim 15, Uchida and Carmichael taught the invention substantially as claimed, including the apparatus as cited in the rejections of claims 1, and 13-14 wherein Uchida was used as a reference. Uchida and Carmichael did not specifically teach wherein said characteristics comprise one or more characteristics selected from the group consisting of volatility, price, and density. However, Wegner taught the cost characteristic [col. 1, lines 14-28]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida, Carmichael, and Wegner because adding Wegner's cost characteristic to Uchida and Carmichael's would improve Uchida and Carmichael's additional device ID information for the purpose of identifying features of the of similar devices [see Wegner, col. 1, lines 14-20].

29. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over "Applicant's Admitted Prior Art (hereinafter referred to as AAPA)" in view of "Supplement to IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture" (hereinafter referred to as Supplement).

30. As for claims 16, AAPA taught the invention substantially as claimed, including a method of selecting one of a number of ID codes of a package comprising the steps of:

(a) asserting a first or a second voltage level on one or more pins of said package; and (b) generating said one of a number of ID codes in response to said voltage levels on said one or more pins [specification pg. 1, lines 10-20, pg. 2, and pg. 3, especially lines 6-11].

AAPA did not specifically teach a single die and package combination. However, Supplement taught a single die and package combination [pg. 3, section B.2, pg. 12, fig B-1, and section B.8.2]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA and Supplement because Supplement is an additional revision adding more functionality to the existing IEEE Std 1149.1 (disclosed by AAPA) which improves on the original IEEE Std 1149.1 standard and would further be obvious to one of ordinary skill in the art to utilize published IEEE standards for the development of additional device functions taught by the IEEE standard.

31. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over "Applicant's Admitted Prior Art (hereinafter referred to as AAPA)" in view of "Supplement to IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture" (hereinafter referred to as Supplement), and further in view of IBM TDB Publication, "Using a portion of the boundary register as the identification register" (hereinafter referred to as IBM).

32. As for claim 17, AAPA and Supplement taught the invention substantially as claimed, including the method of selecting one of a number of ID codes as cited above in the rejection of claim 16 where the AAPA and Supplement references are used. AAPA further taught wherein step (b) comprises the substeps of:

(b-1) determining said voltage levels [pg. 3, lines 9-10, note that because bit levels are used, a determination of voltage levels is taught];

(b-2) determining a state of one or more metal options [pg. 1, lines 19-20, and pg. 3 lines, 7-10, the production of a unique id includes a determination];

(b-3) determining a state of one or more bond options [pg. 3 lines, 7-10 the production of a unique id includes a determination].

AAPA did not specifically teach (b-4) generating an ID code in response to a logical combination of the determination of sub-steps (b-1) through (b-2). However, IBM taught generating an ID code in response to a logical combination of the determination sub-steps (b1) – (b2) [fig. 4 "combination of boundary scan/device ID register"]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA, Supplement, and IBM because AAPA, Supplement, and IBM all utilize the device ID register from the test access port and boundary scan architecture which is in the same field of endeavor. Furthermore, the addition of the logical combination would improve AAPA and Supplements method by reducing circuitry needed and help with distinguishing manufacturers of devices [see IBM pg. 262-263 "pg 2 of the East printout of the article"]

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pederson 5,796,267 logic levels, voltage levels, source, ground

Ma	5,570,042	logic levels, voltage levels
Monti	5,557,236	logic levels, different voltage levels

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy Whitmore
July 12, 2002

PATENT EXAMINER
AU 2812